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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,686	10/23/2001	Ken-Ming Li	372582-00201	7296

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

K.D.

Office Action Summary	Application No.	Applicant(s)	
	10/032,686	LI ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-18, 22-24, 28-30, 34-36 and 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,838,204 to Yao.

Regarding claim 1, Yao (figures 8-10) teaches an integrated circuit comprising:

a power supply I/O pad (a portion of 606);

an I/O pad (a portion of 606) of a first type made of a deposited conductor, wherein the I/O pad (606) of the first type is connected to a first point on an integrated circuit; and

a strip (another portion of 606) of deposited conductor substantially adjacent to the I/O pad (606) of the first type, wherein the strip of disposed conductor is connected to a second point on the integrated circuit.

Yao differs from the claimed invention by not showing the I/O pad of the first type is narrower than the power supply I/O pad so as to allow space for the strip. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the I/O pad of the first type is narrower than the power supply I/O pad so as to allow space for the strip, since the power provides more power to the device.

Regarding claim 2, Yao teaches the I/O pad (606) of the first type is a data I/O pad.

Regarding claim 3, Yao teaches the first point on the integrated circuit is further connected to a circuitry.

Regarding claim 4, Yao teaches the first point on the integrated circuit is further connected to a power bus (608).

Regarding claim 5, Yao teaches the second point on the integrated circuit is further connected to a circuitry.

Regarding claim 6, Yao teaches the second point on the integrated circuit is further connected to a power bus (608).

Regarding claim 7, Yao teaches the strip (another portion of 606) of conductor is connected to a third point on the integrated circuit.

Regarding claim 8, Yao teaches the second and third points on the integrated circuit are connected to a circuitry.

Regarding claim 9, Yao teaches the second and third points on the integrated circuit are connected to a power bus (608).

Regarding claim 10, Yao teaches an I/O pad of the second type (a next portion of the first type of I/O pad [606]) made of a deposited conductor, wherein the I/O pad of the second type is connected to a third point on the integrated circuit.

Regarding claim 11, Yao teaches the I/O pad (a next portion of the first type of I/O pad [606]) of the second type is a data I/O pad.

Regarding claim 12, Yao teaches the third point on the integrated circuit is further connected to a circuitry.

Regarding claim 13, Yao teaches the third pint on the integrated circuit is further connected to a power bus (608).

Regarding claim 14, Yao teaches the strip (another portion of 606) of deposited conductor is connected to a fourth point on the integrated circuit.

Regarding claim 15, Yao teaches the second, third and fourth points on the integrated circuit are connected to a circuitry.

Regarding claim 16, Yao teaches the second, third and fourth points on the integrated circuit are connected to a power bus (608).

Regarding claim 17, Yao teaches the I/O pad (a portion of 606) of the first type provides power to a core circuitry (602).

Regarding claim 18, Yao teaches the power bus (608) is configured as an intersecting grid of a deposited conductor.

Regarding claim 22, Yao (figures 8-10) teaches an integrated circuit comprising:

a power supply I/O pad (a portion of 606) made of a deposited conductor;

a power bus (608) connected to the power supply I/O pad (a portion of 606);

a data I/O pad (other portion of 606) made of a deposited conductor;

circuitry connected to the data I/O pad (other portion of 606); and

a strip (another portion of 606 than I/O pad) of deposited conductor substantially adjacent to the data I/O pad (other portion of 606) wherein the strip of deposited conductor is connected to multiple points (multiple points portions of another portion of 606) on the power bus (608).

Yao differs from the claimed invention by not showing the data I/O pad is narrower than the power supply I/O pad so as to allow space for the strip. It would have been obvious to one

having ordinary skill in the art at the time the invention was made for the data I/O pad is narrower than the power supply I/O pad so as to allow space for the strip, since the power provides more power to the device.

Regarding claim 23, Yao teaches the power bus (608) provides power to a core circuitry (602).

Regarding claim 24, Yao teaches the power bus (608) is configured as an intersecting grid of a deposited conductor.

Regarding claim 28, Yao (figures 8-10) teaches an integrated circuit comprising:

a power supply I/O pad (a portion of 606) made of a deposited conductor;

a power bus (608) connected to the power supply I/O pad (a portion of 606);

a multi-level voltage I/O pad (two portion layers of 606) made of a deposited conductor;

circuitry connected to the multi-level voltage I/O pad (other portion of 606); and

a strip (another portion of 606 than I/O pad) of deposited conductor substantially adjacent to the multi-level voltage I/O pad (two portion layers of 606) wherein the strip of deposited conductor is connected to multiple points (multiple points portions of another portion of 606) on the power bus (608).

Yao differs from the claimed invention by not showing the data I/O pad is narrower than the power supply I/O pad so as to allow space for the strip. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the data I/O pad is narrower than the power supply I/O pad so as to allow space for the strip, since the power provides more power to the device.

Regarding claim 29, Yao teaches the power bus (608) provides power to a core circuitry (602).

Regarding claim 30, Yao teaches the power bus (608) is configured as an intersecting grid of a deposited conductor.

Regarding claim 34, Yao (figures 8-10) teaches an integrated circuit comprising:

a positive power supply I/O pad (a portion of 606) made of a deposited conductor;

a positive power bus (608) connected to the positive power supply I/O pad (a portion of 606);

a data I/O pad (another portion of 606) made of a deposited conductor;

circuitry connected to the data I/O pad (other portion of 606);

a first strip (another portion of 606 than I/O pad) of deposited conductor substantially adjacent to the data I/O pad, wherein the strip of deposited conductor is connected to multiple points (multiple points portions of another portion of 606) on the positive power bus (608); and

It is inherent that a negative power supply I/O pad made of a deposited conductor will be taught in the Yao because they will provide a negative power supply I/O and positive power supply I/O for the operation of the circuit.

It is inherent that a negative power bus connected to the negative power supply I/O pad will be taught in the Yao because they will provide a negative power bus and the positive power bus for the operation of the circuit.

a second strip (second row of the portion of 606) of deposited conductor substantially adjacent to the data I/O pad (another portion of 606), wherein the second strip of deposited

conductor is connected to multiple points (multiple points portions of another portion of 606) on the negative power bus (608).

Yao differs from the claimed invention by not showing the data I/O pad is narrower than the power supply I/O pad so as to allow space for the first and second strip. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the data I/O pad is narrower than the power supply I/O pad so as to allow space for the first and second strip, since the power provides more power to the device.

Regarding claim 35, Yao teaches the power buses (608) provide positive and negative power to a core circuitry (602).

Regarding claim 36, Yao teaches the power buses (608) are configured as intersecting grids of a deposited conductor.

Regarding claims 49-52, the combined device shows the power bus is configured as an intersecting grid of a deposited conductor.

3. Claims 19-21, 25-27, 31-33 and 37-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,838,204 to Yao in view of US Patent No. 6,407,939 to Merritt.

Regarding claim 19, Yao differs from the claimed invention by not showing the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. However, Merritt (figures 2-6) teaches the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. Therefore, it would have been obvious to

one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merritt into the device taught by Yao because it provides interconnection between the layers in the integrated circuit. The combined device shows the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers.

Regarding claim 20, the combined device shows the power bus exists at a lowest layer.

Regarding claim 21, the combined device shows the power bus exists at a second to lowest layer.

Regarding claim 25, Yao differs from the claimed invention by not showing the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. However, Merritt (figures 2-6) teaches the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merritt into the device taught by Yao because it provides interconnection between the layers in the integrated circuit. The combined device shows the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers.

Regarding claim 26, the combined device shows the power bus exists at the lowest layer.

Regarding claim 27, the combined device shows the power bus exists at the second to the lowest layer.

Regarding claim 31, Yao differs from the claimed invention by not showing the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. However, Merritt (figures 2-6) teaches the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merritt into the device taught by Yao because it provides interconnection between the layers in the integrated circuit. The combined device shows the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers.

Regarding claim 32, the combined device shows the power bus exists at the lowest layer.

Regarding claim 33, the combined device shows the power bus exists at the second to the lowest layer.

Regarding claim 37, Yao differs from the claimed invention by not showing the integrated circuit is comprised of multiple metal layers, and wherein the positive and negative power buses are deposited on third and fourth layers, respectively. However, Merritt (figures 2-6) teaches the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merritt into the device taught by Yao because it provides interconnection between the layers in the integrated circuit. The combined device shows the integrated circuit is comprised of

multiple metal layers, and wherein the positive and negative power buses are deposited on third and fourth layers, respectively.

Regarding claim 38, Yao differs from the claimed invention by not showing the integrated circuit is comprised of multiple metal layers, and the positive and negative power supply I/O pads are deposited on a first and second layer, respectively. However, Merritt (figures 2-6) teaches the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merritt into the device taught by Yao because it provides interconnection between the layers in the integrated circuit. The combined device shows the integrated circuit is comprised of multiple metal layers, and wherein the positive and negative power supply I/O pads are deposited on a first and second layer, respectively.

Regarding claim 39, the combined device shows the first and second layers are the same layer.

Regarding claim 40, the combined device shows the negative power bus exists at the lowest layer.

Regarding claim 41, the combined device shows the positive power bus exists at the lowest layer.

Regarding claim 42, the combined device shows the negative power bus exists at the second lowest layer.

Regarding claim 43, the combined device shows the negative and positive power buses are further deposited on a fifth and sixth layer.

Regarding claim 44, the combined device shows the positive power bus exists at the second lowest layer.

Regarding claim 45, the combined device shows the negative power bus exists at the third lowest layer.

Regarding claim 46, the combined device shows the positive power bus exists at the third lowest layer.

Regarding claim 47, the combined device shows the negative power bus exists at the fourth lowest layer.

Regarding claim 48, the combined device shows the positive power bus exists at the fourth lowest layer.

Response to Arguments

Applicant's arguments with respect to claims 1-52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
October 14, 2004

Sara W Crane
Sara Crane
Primary Examiner